between a first and second supply potential, and a centre tap connected with an output terminal of the integrated circuit; and

(b) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal.

2. (Previously Amended) The circuit as claimed in claim 1, wherein a waiting time (t) is provided between the first control pulse and the second control pulse, in which the two pulses do not overlap.

3. (Previously Amended) The circuit as claimed in claim 2, wherein one of the two control pulses is generated from the other of the two control pulses by an inverter delay device.

4. (Previously Amended) The circuit as claimed in claim 1, wherein the first transistor is a P-channel MOS transistor and the second transistor is an N-channel MOS transistor, the control connection of the first transistor being inverted.

5. (Previously Amended) The circuit as claimed in claim 4, wherein the first transistor and the second transistor form a CMOS inverter with independent control gate connections.

6. (Original) A circuit for generating a negative signal pulse in response to receiving a sequence of a positive and negative control pulse, the circuit comprising:

(a) a first transistor including a control terminal and a load path connected between an output terminal and a first supply potential for receiving a negative control pulse at the control terminal;

(b) a second transistor including a control terminal and a load path connected between the output terminal and a second supply potential having a potential less than the first supply potential for receiving a positive control pulse at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and

(c) a pull-up resistor connected between the first supply potential and the output terminal for generating a negative signal pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses.

7. (Original) A circuit according to claim 6 wherein a waiting time is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap.

8. (Original) A circuit according to claim 6 further including an inverter delay device for generating one of the first and second control pulses from the other of the two control pulses.

9. (Original) A circuit for generating a positive signal pulse in response to receiving a sequence of a positive and negative control pulse, the circuit comprising:

(a) a first transistor including a control terminal and a load path connected between an output terminal and a first supply potential for receiving a negative control pulse at the control terminal;

(b) a second transistor including a control terminal and a load path connected between the output terminal and a second supply potential having a potential less than the first supply potential for receiving a positive control pulse at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and

(c) a pull-down resistor connected between the second supply potential and the output terminal for generating a positive signal

pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses.

10. (Original) A circuit according to claim 9 wherein a waiting time is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap.

11. (Original) A circuit according to claim 9 further including an inverter delay device for generating one of the first and second control pulses from the other of the two control pulses.

12. (New) A circuit according to claim 1 wherein the first and second transistors include a source and drain, the drain of the first transistor being connected to the drain of the second transistor, the source of the first transistor being connected to the first supply potential, and the source of the second transistor being connected to the second supply potential.

13. (New) A circuit according to claim 6 wherein the first and second transistors include a source and drain, the drain of the first and second transistor being connected to the output terminal, the source of the first transistor being connected to the first supply potential, and the source of the second transistor being connected to the second supply potential.

14. (New) A circuit according to claim 9 wherein the first and second transistors include a source and drain, the drain of the first and second transistor being connected to the output terminal, the source of the first transistor being connected to the first supply potential, and the source of the second transistor being connected to the second supply potential.

REMARKS

I. Status of Claims

Claims 1-11 are currently pending. Claims 12-14 are added. Therefore, upon entry of this Amendment, Claims 1-14 will be pending and under